IN THE CLAIMS:

Please find a listing of the claims below. The statuses of the claims are shown in parentheses.

1-13. (Cancelled)

14. (Original) An on-chip by-pass capacitor comprising:

a first electrode formed during a deposition of a first metal layer of a multi-level deposition device;

a substantially thin dielectric layer configured to be deposited over said first electrode; and

a second electrode formed during a deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is formed over said substantially thin dielectric layer.

15. (Original) The on-chip by-pass capacitor according to claim 14, wherein a dielectric constant of said substantially thin dielectric material layer is substantially high.

16. (Original) The on-chip by-pass capacitor according to claim 15, wherein said substantially thin dielectric material layer includes silicon nitride.

17. (Original) The on-chip by-pass capacitor according to claim 14, wherein said thickness of said substantially thin dielectric material layer is between 50 to 100 angstroms.

18. (Original) The on-chip by-pass capacitor according to claim 14, wherein said substantially thin dielectric material comprises a composite of materials.

19. (Original) The on-chip by-pass capacitor according to claim 18, wherein said composite of materials includes PZT and platinum.

20. (New) The on-chip by-pass capacitor according to claim 14, wherein the first electrode comprises a first electrode formed during the deposition of the first metal layer of a VLSI device.

21. (New) The on-chip by-pass capacitor according to claim 14, further comprising at least one via between the second electrode and the substantially thin dielectric layer.

22. (New) The on-chip by-pass capacitor according to claim 14, further comprising two barrier layers, wherein the substantially thin dielectric layer is positioned between the two barrier layers.

23. (New) The on-chip by-pass capacitor according to claim 14, wherein the first electrode is formed among a plurality of metal signal lines arranged in a parallel line configuration.

24. (New) The on-chip by-pass capacitor according to claim 14, wherein the second electrode is formed among a plurality of metal signal lines arranged in a parallel line configuration.

25. (New) An on-chip by-pass capacitor comprising:

a first electrode;

a substantially thin dielectric layer;

a second electrode; and

at least one via between the second electrode and the substantially thin dielectric layer.

26. (New) The on-chip by-pass capacitor according to claim 25, further comprising:

two barrier layers, wherein the substantially thin dielectric layer is positioned between the two barrier layers.

27. (New) An on-chip by-pass capacitor comprising:

a first electrode formed during a deposition of a first metal layer of a multi-level deposition device;

a substantially thin dielectric layer configured to be deposited over said first electrode;

a second electrode formed during a deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is formed over said substantially thin dielectric layer;

at least one via between the second electrode and the substantially thin dielectric layer; and

two barrier layers, wherein the substantially thin dielectric layer is positioned between the two barrier layers.